

Please add new claim 20 as follows:

A2 Sub C37 20. (New) The electro-optical device according to claim 1, wherein portions of the plurality of scanning lines form the gate electrodes.

REMARKS

Claims 1-20 are pending. Claims 9-19 have previously been withdrawn from consideration. By this Amendment, claims 2 and 3 are amended, claim 20 is added and Figs. 4 and 5 are corrected pursuant to the attached Request for Approval of Drawing Corrections.

Reconsideration based on the following Remarks is respectfully requested.

The attached Appendix includes marked-up copies of each rewritten claim (37 C.F.R. §1.121(c)(1)(ii)).

I. The Drawings Satisfy All Formal Requirements

The Office Action objects to the drawings based on informalities. Figs. 4 and 5 are corrected pursuant to the attached Request for Approval of Drawing Corrections to obviate this objection. Withdrawal of the objection to the drawings is respectfully requested.

II. The Claims Satisfy All Requirements Under 35 U.S.C. §112, Second Paragraph

The Office Action rejects claims 2 and 3 under 35 U.S.C. §112, second paragraph as being indefinite. Claims 2 and 3 are amended to obviate this rejection. Withdrawal of the rejection under 35 U.S.C. §112, second paragraph is respectfully requested.

III. The Claims Define Patentable Subject Matter

The Office Action rejects claims 1 and 3-7 under 35 U.S.C. §102(b) over Nakazawa et al. (U.S. Patent No. 5,614,730); and claims 2 and 8 under 35 U.S.C. §103(a) over Nakazawa et al. in view of one of ordinary skill in the art. These rejections are respectfully traversed.

Nakazawa et al. does not disclose an electro-optical device including, inter alia, at least one portion of ends in the gate width direction of gate electrodes forming transistors being disposed in a semiconductor region forming the transistor, and ends in the gate length direction of each of the gate electrodes extending outside of the semiconductor region forming the transistor, as recited in claim 1.

Instead, according to the active matrix substrate of Nakazawa et al., the one end in the gate width direction of the gate electrodes are disposed outside of the semiconductor region, and the end in the gate length direction of the gate electrodes are arranged inside of the semiconductor region. See, for example, Fig. 1A of Nakazawa et al.

The knowledge of one having ordinary skill in the art would not make up for the deficiencies of Nakazawa et al. Thus, even combining the knowledge of one having ordinary skill in the art with Nakazawa et al. would not result in the invention as recited in claim 1.

For at least these reasons, it is respectfully submitted that claim 1 is patentable over Nakazawa et al. Claims 1-8 are likewise patentable over Nakazawa et al. for at least the reasons discussed as well as for the additional features they recite. Applicant respectfully requests that the rejections under 35 U.S.C. §102 and §103 be withdrawn.

IV. Conclusion

In view of the foregoing, Applicant respectfully submits that this application is in condition for allowance. Favorable consideration and prompt allowance are earnestly solicited.

APPENDIX

Changes to Claims:

Claim 20 is added.

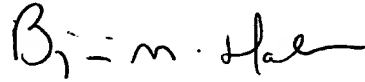
The following is a marked-up version of the amended claims:

2. (Amended) The electro-optical device according to claim 1, ~~a~~the
semiconductor layer forming the transistor comprising monocrystalline silicon.

3. (Amended) The electro-optical device according to claim 1, ~~a~~the
semiconductor layer forming the transistor comprising polycrystalline silicon.

Should the Examiner believe anything further is desirable in order to place this application in even better condition for allowance, the Examiner is invited to contact Applicant's undersigned representative at the telephone number listed below.

Respectfully submitted,



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JAO:BMH/gpn

Attachments:
Appendix
Request for Approval of Drawing Corrections

Date: January 18, 2002

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